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B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2007.

Third Semester

(Regulation 2004)

Computer Science and Engineering

CS 1202 – DIGITAL PRINCIPLES AND SYSTEMS DESIGN

(Common to Information Technology)

(Common to B.E. (Part-Time) Second Semester Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are error detecting codes?

2. Find the complements for the following functions

   (a) $F_1 = xy' + x'y$

   (b) $F_2 = (xy + y'z + xz)x$

3. Draw the circuit diagram for 3 bit parity generator.

4. What are the drawbacks of K-Map method?

5. What is logic synthesis in HDL?

6. When an overflow condition will encounter in an accumulator register?

7. What is gate level modeling?

8. What are the differences between sequential and combinational logic?

9. Draw the logic diagram for D-Type Latch.

10. What are the assumptions made for pulse mode circuit?

PART B — (5 × 16 = 80 marks)

11. (a) Using Tabulation method simplify the Boolean function

$F(w,x,y,z)=\Sigma(2,3,4,6,7,11,12,13,14)$ which has the don't care conditions $d(1,5,15)$.

Or

(b) Simplify the Boolean function using Variable Entered Mapping method and implement using gates

$F(w,x,y,z)=\Sigma(0,2,4,6,8,10,12,14)$.

12. (a) (i) Design a combinational circuit to convert gray code to BCD. (12)

(ii) Design a Full adder circuit with a Decoder. (4)

Or

(b) Design a 4 bit magnitude comparator to compare two 4 bit numbers.

13. (a) Implement the Boolean function using 8 : 1 multiplexer

$F(A,B,C,D)=AB'D+A'C'D+B'C'D+AC'D$.

Or

(b) Explain the different types of ROM.

14. (a) Construct a full subtractor circuit and write a HDL program module for the same.

(i) Compare synchronous with Asynchronous counters. (8)

(ii) Explain the behavioral Model with suitable example. (8)

Or

(b) (i) A positive edge triggered flip-flop has two inputs D_1 and D_2 and a control input that chooses between the two. Write an HDL behavioral description of this flip-flop. (8)

(ii) Construct and explain 4 stage Johnson counter. (8)

15. (a) (i) Explain the need for key debounce circuit. (8)

(ii) What is the objective of state assignment in asynchronous circuit? Give hazard-free realization for the following Boolean functions

$$F(A,B,C,D)=\Sigma M(0,1,5,6,7,9,11)$$ (8)

Or

(b) An asynchronous sequential circuit is described by the following excitation and output function

$$B=(A_1'B_2)B+(A_1+B_2)$$

$$C=B$$

(i) Draw the logic diagram of the circuit. (5)

(ii) Derive the transition table and output map. (6)

(iii) Describe the behavior of the circuit. (5)